A 0.18 μm CMOS Digitally Controlled Oscillator for Closed-Loop Modulation Systems

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Abstract—This paper addresses the design and implementation of a digitally controlled oscillator (DCO) as a possible step towards an all-digital closed-loop modulation implementation for DECT applications. Based on a complete transmitter system model a simplified model describing only the modulation is developed. Simulations based on this system shows that a simple 5 bit modulator is sufficient for achieving the required modulation accuracy. The complete system is tested and measured using a prototype chip. The DCO design uses a standard 6 metal layer 0.18 μm CMOS technology. The experimental results show that the achieved modulation performance complies with the DECT specifications. The design can be extended for compliance with other frequency modulation systems such as GSM, Bluetooth, DCT, WLAN etc.

I. INTRODUCTION

The typical low-cost FSK transmitter makes uses of open-loop modulation. An alternative implementation strategy is to make use of closed-loop modulation instead. This option has generally been rejected due to the inherent increase in both complexity and cost. Lately, different closed-loop topologies have been proposed for low-cost applications such as DECT and Bluetooth [1], [2], [3]. For Bluetooth applications an all-digital solution has been proposed and a prototype design using very sophisticated technology shows that the Bluetooth standard is complied with [3]. As an example, the reference frequency for the ΣΔ-modulation is set to 600 MHz which makes the system power inefficient. In this work the DECT standard is chosen as target application.

One of the major benefits of an open-loop modulation topology is that it is fairly simple to implement. However, when the complete system, including the synthesizer PLL, is integrated problems start to occur. For instance, when the loop is open and no feedback control therefore is present frequency pushing and pulling result. This often requires extra off-chip isolation between RX/TX which require more off-chip components. As a result of such issues most solutions based on a cheap open-loop transceiver chip eventually result in an increased bill of material. The pitfalls of using open-loop modulation are thus primarily caused by two factors; i) the lack of feedback control during modulation and ii) interfacing between off-chip and on-chip components. One way to mitigate many of the pitfalls of open-loop modulation systems is to make use of single-chip closed-loop modulation systems. By keeping the loop closed any phase shifting due to pushing and pulling effects are compensated by the loop.

As a further tool for improving robustness a DCO may be used in stead of a traditional VCO. This way a digital on-chip loop-filter can be used whis mitigates the effects of component tolerances on loop filter related performance. This also reduces the amount of critical interfacing between off-chip and on-chip components. As a further note, a closed-loop system offers the possibility to use an entirely new receiver topology, coherent detection, as opposed to the traditionally used low IF receiver. This has the potential of improving the sensitivity of the final application.

In this work a simplified closed-loop design is presented. The design is based on a Digital Phase Locked Loop (DPLL) with modulation feed at the VCO input. The modulation is removed after the DCO by controlling the division ratio through a ΣΔ-modulator. The result is that the modulation is unaffected by the loop as intended. The modulation is examined in time and frequency domain. This ends up with a simplified open loop model as shown in Fig. 1. To minimize pushing and pulling effects from the front-end the DCO runs at double the frequency from normal European DECT systems. This requires overmodulation by a factor of two which is applied at the DCO’s digital modulation input.

II. SYSTEM REQUIREMENTS

The DECT system has a total frequency spectrum allocation of 20 MHz. The European frequency spectrum extends from 1880 MHz to 1900 MHz and this is the frequency band used for this work. The allocation is divided into 10 carriers separated by 1.728 MHz. The channel frequency equation is

\[ F_c = 1897.344 - c \times 1.728 \quad [\text{MHz}] \quad (1) \]

In order to reduce the bandwidth of the modulated signal the digital bit stream is shaped using a Gaussian filter with a Bandwith Time (BT) of 0.5.
During transmission in successive frames the adjacent channel power must be less than the values shown in Figure 2. These are called emission due to modulation requirements. \( M \) in Fig. 2 is the RF channel used to transmit the packet. As \( Y \) is any DECT channel more than 3 channels away from \( M \), the maximum power level must be less than \(-44\) dBm/MHz except for one instance of a 500 nW signal [4].

One of the key parameters in designing the DCO is the bit resolution at the modulation input of the oscillator. To determine the required number of bits a series of simulations is performed to provide a relation between Power Spectral Density (PSD) and the number of bits. For each bit resolution a random sequence of approximately 2 million bits is sent through the simulation system. Based on such simulations a PSD is produced and on top of this phase noise is added based on Leeson’s formula and an assumed inductor quality factor \( Q \) of 8. During simulations an Additive White Gaussian Noise (AWGN) channel is assumed. A relevant sample of the results can be seen in Figure 3, where the PSD’s are plotted for comparison.

As seen from Figure 3 the quantization noise is mostly buried in the noise floor for resolutions of 4 bits and above. This means that the effect of having higher resolution is negligible. Fewer bits at the input of the DCO gives a less complicated system which is desired. When using a 4 bit input the quantization noise meets the emission mask. Due to process variations and nonlinearities in the design the peak frequency deviation of the oscillator must be designed with a significant implementation margin. As a result the peak frequency deviation is chosen to be 50% larger than \( \pm 576 \) kHz at the direct output of the DCO which corresponds to 3.8 GHz. To accommodate this extra margin an additional bit is added to the modulation. This leads to a resulting quantization level of 5 bit.

### III. CIRCUIT DESIGN

A prototype design of the DCO is produced in a standard digital 0.18 \( \mu \)m CMOS process with 6 metal layers and thick top metal. The DCO is implemented as a standard single-inductor differential LC-oscillator with a head current source. A simplified schematic is shown in Fig. 4.

![Block diagram of the DCO](image)

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![Block diagram of the DCO](image)

The digital converter is used to convert the 5 bit Frequency Tuning Word (FTW) at the modulation input port to 32 bit thermometer code. The main motivation for using thermometer coding to control the capacitor bank is to prevent instantaneous opposite shift of capacitors. If the varactors shift in a binary manner it causes some to shift from high to low state while others at the same time shift from low to high state. That leads to positive and negative transients in the output frequency response which again leads to problematic spurious emission in the output spectrum.

![Block diagram of the DCO](image)
The capacitor bank is shown in Fig. 5. A large fixed interdigital capacitor (IDCAP) utilizing vertical and lateral flux, \( C_{\text{par}} \), is used to set the center frequency of the oscillator. For modulation, each step in FTW is applied using a varactor pair, \( C_{\text{var}} \). With 5 bit resolution the maximum frequency deviation of 2.576 kHz is represented by 32 steps of 36 kHz each. This is not directly achievable with the CMOS process used, so series capacitances, \( C_{\text{ser}} \), are added to the tank for lowering the step size. For linearizing the capacitance versus FTW curve, a parallel IDCAP, \( C_{\text{lin}} \), is added across the varactors. To comply with production inaccuracies by a coarse frequency shift, coarse tuning varactors, \( C_{\text{coarse}} \), are added.

![Fig. 5. Structure of the tank capacitance. 32x\( C_{\text{var}} \) are the 32 varactors. 2x\( C_{\text{coarse}} \) are the two coarse tuning varactors.](image)

The digital capacitance levels are created by shifting between high and low capacitance states for 32 NMOS varactor pairs. The high and low states are found in the depletion and accumulation regions of the varactor pairs. In order to compensate for matching issues, all varactors in the varactor bank are identical and laid out with dummy varactors surrounding all sides of the bank. When using capacitances in series to the tank nodes, \( C_{\text{ser}} \), the FTW to frequency response slope gets more non-linear. Therefore a predistortion of the FTW is worth investigating to linearize the FTW to frequency response.

To find \( C_{\text{ser}} \) a simplified model for the modulation capacitance is developed - this is found in Figure 6. \( C_{\text{1, min}} \) is the parallel connection of \( C_{\text{lin}} \) and the 32 varactors in low capacitance state. \( \Delta C_1 \) is the capacitance step occurring when all varactors are shifted from low to high capacitance state. \( C_2 \) is the series connection of the two serial capacitances and \( C \) is the total capacitance at the tank nodes.

![Fig. 6. Simplified model for the modulation capacitance.](image)

The tank node maximum and minimum capacitances, \( C_{\text{max}} \) and \( C_{\text{min}} \), are calculated from the known inductance of 1 nH and the wanted output frequency limits. From that an expression for \( C_2 \) is derived

\[
C_{\text{max}} = C_{\text{min}} + \Delta C = \frac{(C_{\text{1, min}} + \Delta C_1)C_2}{C_{\text{1, min}} + \Delta C_1 + C_2} = \frac{C_{\text{1, max}}C_2}{C_{\text{1, max}}C_2 - (C_{\text{min}} + \Delta C)} \\
\downarrow \\
C_2 = \frac{C_{\text{1, max}}(C_{\text{min}} + \Delta C)}{C_{\text{1, max}} - (C_{\text{min}} + \Delta C)}
\]

\[
C_{\text{min}} = \frac{C_{\text{1, min}}C_2}{C_{\text{1, min}} + C_2} \\
\downarrow \\
\Delta C_1C_{\text{min}}^2 + \Delta C_1C_{\text{min}} + \Delta C C_{\text{1, max}}C_{\text{1, min}} = 0
\]

\[
C_{\text{min}} = -\frac{\Delta C \Delta C_1}{2\Delta C_1} ± \sqrt{(\Delta C \Delta C_1)^2 - 4\Delta C^2 \Delta C C_{\text{1, max}}C_{\text{1, min}}} \quad (2)
\]

If DEV in percentage represents the production deviation due to inaccuracies, the series and parallel capacitances can be calculated as:

\[
C_{\text{ser}} = (1 \pm \text{DEV}) \frac{C_1C_{\text{min}}}{(C_1 - C_{\text{min}})} \quad (3)
\]

\[
C_{\text{par}} = C_{\text{center}} - C_{\text{min}} \quad (4)
\]

The capacitor bank design is crucial for the functional performance of the DCO and this is therefore chosen to be the main focus of the work.

IV. RESULTS

The designed DCO is produced in a 32 pin LLP package prototype chip. The chip is tested on the test board depicted in Figure 7. The test board has a connector for off-board control of the digital inputs. An FPGA is used for generating these signals. The differential output of the DCO is converted to a single ended signal through a balun and sent to SMA connectors both directly and through a divider that sends out the normal DECT frequency. The evaluation of the DCO performance is done by measurements with the prototype chip on the test board.
The distortion of the FTW to frequency deviation curve is found by sweeping the FTW from 0b11111 to 0b00000 and demodulating the output. Each FTW must be sustained sufficiently long for the system to settle. Fig. 8 shows the distorted and predistorted curves. The lower ramp-up response is the distorted frequency to FTW relation and it is clear that the relation initially is not linear. By making a polynomial fitting of the distorted curve and filter the ramp through a compensating polynomial, the dashed curve in Fig. 8 appears. Thus, from a modulation point of view, the predistortion principle works in practice in time domain. But it is also clear that the result is not smooth with equal step sizes. This is due to the fact that only the Integral Non-Linearity (INL) is compensated for when using the inverse polynomial fitting. The Differential Non-Linearity (DNL) is represented by the difference in step sizes and this has not been compensated for.

As seen in Fig. 10, predistortion also has an effect on the output spectrum, where in this case a random GMSK sequence is transmitted. In particular it evens out the distortion components around 3.5 and 7 MHz. This has a positive effect on the emission due to modulation test because the sidebands are lower. So altogether, predistortion has a positive effect on the output spectrum sidebands and compensates for the in-channel asymmetries caused by the imperfect and distorted FTW to frequency deviation curve.

The amount of noise in the adjacent channels is within the limits given in the DECT requirements. This is stated in Table I.

Finally the DCO is measured when modulating a signal using GMSK as described in the DECT specifications and the output of this test is shown in Fig. 11. The maximum frequency deviation when repeatedly shifting between zeros corresponding to 120 kHz. This overshoot is seen when MSB is shifted due to insufficient on-chip buffering. The settling time is well within the limit of 50 µs set by the DECT specification of the guard space between the transmit slots.
and ones is approximately ± 250 kHz for modulation with predistortion. The long non-shifting sequences result in a maximum frequency deviation of 280 kHz. For the non-pre-distorted modulation quick shifting bits cause frequency deviation of 250 kHz down to -320 kHz, and the maximum is just around -395 kHz which meets the requirements of DECT.

<table>
<thead>
<tr>
<th>Channel</th>
<th>Measured [dBm]</th>
<th>Requirement [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st adjacent</td>
<td>-17.6</td>
<td>-8</td>
</tr>
<tr>
<td>2nd adjacent</td>
<td>-34.1</td>
<td>-30</td>
</tr>
<tr>
<td>3rd adjacent</td>
<td>-41.8</td>
<td>-41</td>
</tr>
</tbody>
</table>

**TABLE I**

**ADJACENT CHANNEL EMISSION REQUIREMENTS COMPARED TO MEASURED POWER WITH A TRANSMIT POWER OF 24 dBM.**

V. Conclusion

It has been shown that digital FSK modulation is implementable in a state of the art 0.18 µm CMOS process using a low 5 bit resolution. A digitally controlled oscillator for DECT has been designed and implemented. In the current version the oscillator is able to modulate a gaussian shaped signal onto a carrier in compliance with the requirements of the DECT specifications. The signal quality requirements can be extended to FSK systems like GSM, Bluetooth, PCT or WLAN using GFSK and thus the application area is significantly widened. The task of tuning the center frequency has been omitted from this study and could be the next step towards a fully functioning all-digital transceiver for low-cost wireless applications.

VI. Discussion

If tuning circuitry is added this result opens up for a new generation of transceiver chips that are superior to the present state of the art models. Compared to the currently used systems the presence of a DCO rather than a VCO opens the possibility to make well defined digital transceivers. This is beneficial for both the transmitter and receiver. In transmission, digital closed loop modulation with better offset and drift control can be achieved. In the receiver, coherent detection can be implemented resulting in better sensitivity performance. It will be easier to integrate the transceiver into an application as the interfaces between off-chip and on-chip components decreases. All together, cheaper systems with a shorter time-to-market may be available if this concepts is made production ready and put onto the market.

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REFERENCES


Dan Dejgaard Sommerlund Hermansen was born in Vejle, Denmark, in 1979. He received his M.Sc. degree in electrical engineering from Aalborg University, Denmark, in 2005. His specialization on making a Digitally Controlled Oscillator was conducted in the department of Communication Technology with the RF Integrated Circuits and Systems group. During his Master studies he has concurrently been working with projects related to the development of low-price and low-complexity closed loop modulation transceivers. During his studies he has been working together with RTX Telecom and SiTel Semiconductor to share knowledge and knowhow in the fields of wireless applications and CMOS chip design and implementation. This cooperation included an internship at SiTel Semiconductor in Hengelo, The Netherlands.

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Emil Feldborg Buskgaard graduated in 2005 as M.Sc. in electrical engineering from Aalborg University, Denmark. During his studies he has focused his attention on design and implementation of low-cost closed-loop transmitter systems suitable for IC production. His work has been supported by RTX Telecom, Denmark, and SiTel Semiconductor, The Netherlands, and covers many aspects of transceiver design both on system level and on circuit level.

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Christian Smit received his B.Sc. in electrical engineering from polytechnic school Hogeschool Enschede, The Netherlands, in 1996. He joined Ericsson as an RF design engineer and worked on DECT and the first generation Bluetooth transceivers. Focus of his work was mainly frequency synthesis design. In 2000 he joined National Semiconductor and continued working on frequency synthesizer design for DECT and DCT transceivers. Currently the DECT group has been sold and continues as an independent company named SiTel Semiconductor BV.

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From 1993 to 1995 he worked at the Space Research Organization of the Netherlands (SRON) and contributed to the ESA-XMM satellite project. From 1995 to 1999 he worked at Philips Research (Nat-Lab) in the field of integrated (CMOS) transceivers. From 1999 to 2005 he worked at National Semiconductor on the development of RF IC’s for wireless applications. Since 2005, he has been with SiTel Semiconductor, ‘s-Hertogenbosch, the Netherlands, where he currently is working as RF IC development manager.

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Poul Olesen received his M.Sc. degree in electrical engineering from Aalborg University, Denmark, in 1988. His field of specialization was to make a front-end for cordless phones from the department of Communication Technology.

He has worked with design and RFIC solutions for cell phones and cordless phones for various companies and customers: Dancall Telecom A/S, Bang&Olusen, Rockwell Semiconductor Systems and RTX Telecom A/S. Poul Olesen has worked with all aspects of RF and system design such as RFIC system design and application for DECT, 2.4 and 5.8 GHz DCT, WLAN, GSM as well as medical applications. Currently he is coordinating the RF activities within the Cordless RF team at RTX as well as co-supervising student projects at Aalborg University.

Finn Helsgaard Andreasen

Finn Helsgaard Andreasen (M’94) received his M.Sc. degree in electrical engineering from Aalborg University, Denmark, in 1994. His specialization study was in the field of robust bit synchronization for DECT from the department of Telecommunications.

He has been with Dancall Telecom from 1994. In 1996 he joined RTX Telecom A/S, Denmark, where he is now working as Senior Group Coordinator for the RF group. He has mainly been working in the field of Cordless phone technologies such as DECT, 2.4 GHz DCT and 5.8 GHz. He has also been involved in RF design of 802.11 a/b/g radios.

Torben Larsen

Torben Larsen was born in Nrresundby, Denmark, in 1964. He received the M.Sc. degree in electrical engineering from Aalborg University, Denmark, in 1988, and the Doctor Technices degree from the same university in 1998. Torben Larsen has worked in various positions at Aalborg University, and at the companies Bosch Telecom and Siemens Mobile Phones. Torben Larsen has been employed as full professor at Aalborg University since 2001. He has formed and is leading a research group working on RF Integrated Systems and Circuits which currently counts 15 researchers and teachers.

Torben Larsen is senior member of IEEE, and serves as reviewer for IEE and IEEE magazines and transactions and for a number of conferences. He has been a member of the steering committee for the European Microwave conference from 1999 to 2001. He is member of the NORCOM board which is an entity of roughly 20 companies and Aalborg University coordinating various activities in the wireless area. Torben Larsen received the 250.000 DKK Spar Nord Research Prize in 1999 for excellent research work. He is currently the leader of several major research projects funded by industry, EU and the Danish research ministry on various aspects of wireless communications. In 2005 Torben Larsen was appointed by the Danish minister of science, technology and innovation to be member of the research council for technology and production.

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